This Page Is Inserted by IFW Operations and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents will not correct images, please do not report the images to the Image Problem Mailbox.



DOCKET NO.: 24061.42 (TSMC2002-1015)

CUSTOMER NO.: 27683

INVENTOR'S DECLARATION FOR PATENT APPLICATION

As below named inventors, we hereby declare that:

Our residence, post office address and citizenship are as stated below next to our names;

We believe we are the original, first and sole joint inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled

SEMICONDUCTOR WAFER MANUFACTURING METHODS EMPLOYING CLEANING DELAY PERIOD

the specification of which was filed on November 13, 2003 under Attorney's Docket Number 24061.42 (TSMC2002-1015) as Application Serial No. 10/712,460.

We hereby state that we have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

We acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C.1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF INVENTOR: Chia-Lin Chen

INVENTOR'S SIGNATURE: Chia-Lin Chen

DATED: 35/13 /04

RESIDENCE: Hsin-Chu, Taiwan, R.O.C.

POST OFFICE ADDRESS: 5f, no. 111, Minshiang St.

No.8 Allow ≥3, Lane 15≥, Soc. 2, Jungshing

Hsin-Chu, Taiwan 300 Republic of China

Rd., Judung Jen, Heinchu, Taiwan 310,

CITIZENSHIP: Taiwan, R.O.C.

R. O.C

DOCKET NO.: 24061.42 (TSMC2002-1015)

CUSTOMER NO.: 27683

FULL NAME OF INVENTOR: Tze-Liang Lee

INVENTOR'S SIGNATURE: Ite liang lee

RESIDENCE:

Hsin-Chu, Taiwan, R.O.C.

POST OFFICE ADDRESS:

No. 6, Alley 1, Lane 158 Chang Chuen Street Hsin-Chu, Taiwan 300 Republic of China

CITIZENSHIP: Taiwan, R.O.C.

FULL NAME OF INVENTOR: Shih-Chang Chen

lith-Chang Chen DATED: 05/13/04

RESIDENCE:

Hsin-Chu, Taiwan, R.O.C.

POST OFFICE ADDRESS:

5f, no. 111, Minshiang St.
Hsin-Chu, Taiwan 300
Republic of China

CITIZENSHIP: Taiwan, R.O.C.

5F, No. 970, Sec. 4, Chang-Hising Rd., Chu-Tung. Hsin-Chu, Taiwan, R.O.C.